SLOW-WAVE APPROACH FOR MONOLITHIC Ga-As ICs

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One of the most important things in the MMICs design is to minimize the monolithic circuit size. Microstrip or coplanar line approach, cannot lead to a consistent size reduction because the physical line lengths, for a given electrical length, are not very different in Al_2O_3 and in GaAs.

A second problem which limits the monolithic circuit design, is the reduced characteristic impedance range of the line which can be realized on the GaAs wafer in a reliable and reproducible way, with practical line widths. This prevents, for example, the realization of low-impedance line lengths, which can be very useful in the input or interstage matching networks of medium power FET amplifiers. A third problem which limits, in particular, the design of coplanar waveguide MMICs, is the slot-mode signal propagation. The slow-wave circuit approach, which uses transmission line lengths periodically loaded with high-Q lumped capacitors[1], could overcome all the limitations mentioned above.

This paper will report:

a) the experimental and the computed results concerning the frequency behavior of slow-wave structures over semiinsulating GaAs;
b) the design and the performances of a medium power monolithic amplifier, using an interstage matching network with a slow-wave structure (having an equivalent characteristic impedance of 20 Ω);
c) the design criteria and the measured performances of various type of slow-wave elements for monolithic GaAs circuits (e.g. directional coupler of various types) which allows substantial chip size reductions.

Additional supporting material:

The basic concepts of the slow-wave structures will be presented first. Then the measured transmission and reflection coefficients of some typical slow-wave structures in a 50 Ω test jig (see figs. 1 and 2) will be compared with those calculated for an equivalent transmission line and those of a computer simulation of the slow-wave structures. The frequency limits of the various kinds of structures, will be outlined. Then, various circuit examples, which demonstrate the usefulness of the proposed structure to solve the problems listed in the abstract, will be reported. As a first example, the design and the performances of a 20 dB gain, medium power, two stage, monolithic amplifier will be described. This circuit make use of 1 μm gate length ion implanted FET devices. The gate width are 600 μm and 1200 μm respectively for the first stage and the second stage device.

The total chip area is 3.2x2.4 mm^2. Fig. 3 gives the small signal gain as a function of the frequency. As can be seen by the basic amplifier circuit, reported in fig. 4, the interstage matching network, make use of a quite long line length with a characteristic impedance of 20 Ω. Using a 120 μm thick GaAs substrate, the width of a microstrip with such characteristic impedance should be about 500 μm. Using a coplanar waveguide with a ground plane[2] the resulting slot width should be too low, for practical total line width. Using the slow wave approach we were able to reduce the total line width to less than 100 μm, reducing also the physical length of the line for a factor >2.

As further examples the design and the performances of various type of directional couplers will be reported, where the save of the line length as well as of the total chip area has proven to be very high. In figs. 5 and 6 the picture and the performance of a -3 dB, quarter wavelength slow-wave coupler are reported.

(1) E. M. Bastida, G. P. Donzelli: Periodic Slow-wave low-loss structures for monolithic GaAs microwave circuits. Electr. Lett. 15, no. 19 (1979).

(2) R. A. Pucel: "Design considerations for monolithic microwave circuits", IEEE Trans., MTT-29, no. 6, June 1981.

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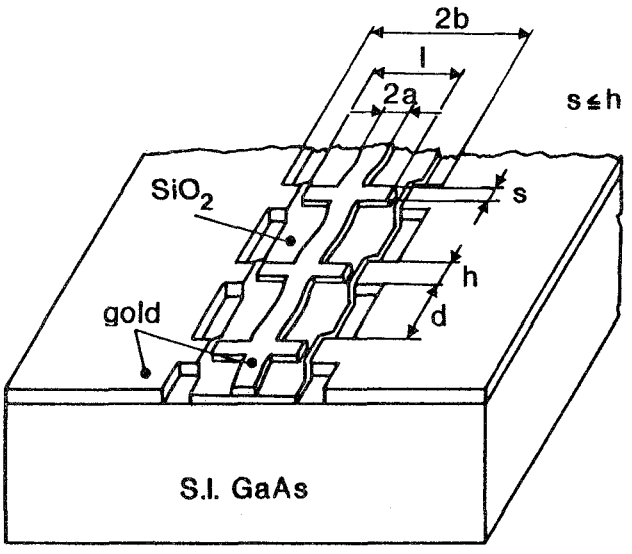


Fig. 1 Depiction of a slow-wave structure processed on GaAs.

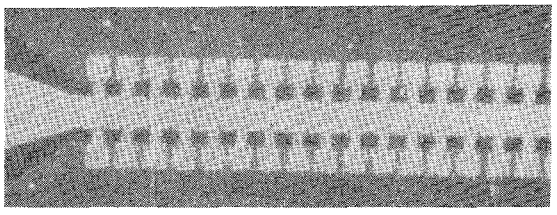


Fig. 2 Photograph of 50Ω slow-wave structure.

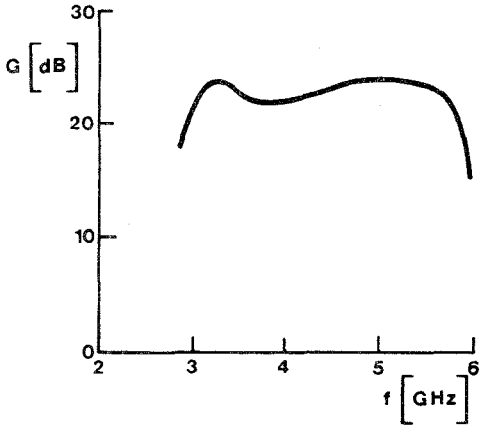
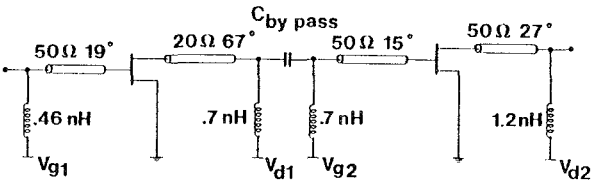


Fig. 3 Small-signal gain versus frequency characteristic for a two-stage monolithic amplifier.



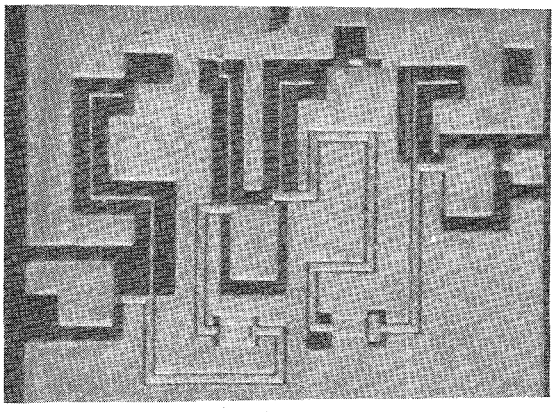


Fig. 4 Circuit representation for two-stage monolithic amplifier.

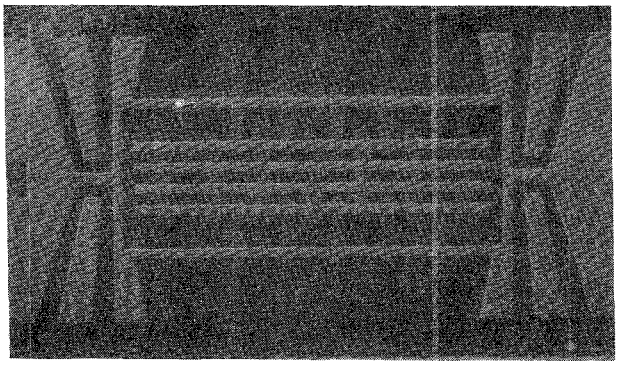


Fig. 5 Circuit layout for slow-wave 3 dB coupler.

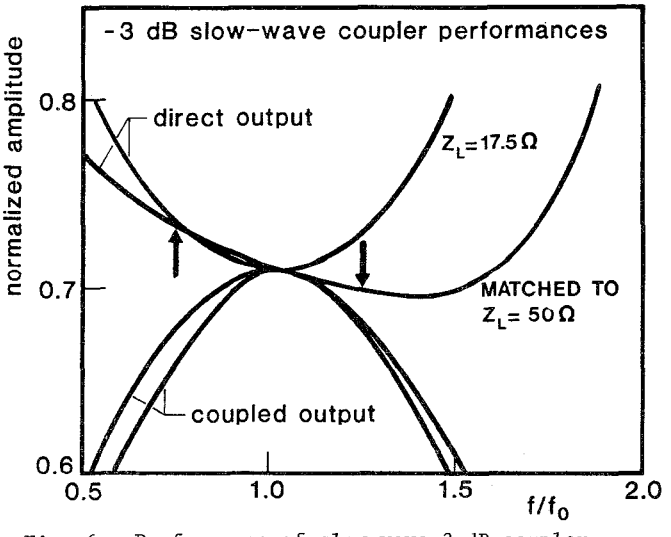


Fig. 6 Performance of slow-wave 3 dB coupler.